WHAT IS CLAIMED IS:

1. A circuit, comprising a comparator having an output and a pair of inputs, wherein the pair of inputs are adapted to receive an output signal produced from the circuit and a reference voltage forwarded to the circuit, and wherein the output is coupled to a pull-down transistor that is connected to one of the pair of inputs.

2. The circuit as recited in claim 1, wherein said one of the pair of inputs is coupled to receive the output signal.

3. The circuit as recited in claim 1, wherein the positive input of the pair of inputs is adapted to receive the output signal and the negative input of the pair of inputs is adapted to receive the reference voltage.

4. The circuit as recited in claim 1, wherein the pull-down transistor comprises a gate conductor and a source-to-drain current path formed between said one of the pair of inputs and a ground supply voltage whenever a voltage of the output signal coupled to the gate conductor exceeds the reference voltage.

5. The circuit as recited in claim 1, further comprising a current source coupled in parallel with the pull-down transistor between said one of the pair of inputs and a ground supply voltage.

6. The circuit as recited in claim 1, further comprising a pull-up transistor having a gate conductor and a source-to-drain current path formed between a power supply voltage and said one of the pair of inputs whenever a voltage of an input signal coupled to the gate conductor exceeds a voltage of the output signal by a threshold voltage of the pull-up transistor.

7. A system for adjusting the pulse width of an output signal, comprising:

a circuit for maintaining a reference voltage between the positive and negative voltage peaks of the output signal; and

a comparator coupled to compare a voltage of the output signal to the reference voltage and, depending in part on the slew rate and/or gain of the comparator, for fixing the minimum voltage of the output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage.

8. The system as recited in claim 7, wherein the output signal comprises a duty cycle that varies in proportion to changes in the reference voltage.

9. The system as recited in claim 7, wherein the circuit is adapted to increase the reference voltage and thereby cause a corresponding decrease in the pulse width and a duty cycle of the output signal.

10. The system as recited in claim 7, wherein the circuit is adapted to decrease the reference voltage and thereby cause a corresponding increase in the pulse width and a duty cycle of the output signal.

11. The system as recited in claim 7, wherein the lesser voltages of the output signal are chopped and removed at the reference voltage.

12. The system as recited in claim 7, wherein the slew rate and/or gain of the comparator is predetermined to preclude a voltage of the output signal from being less than the reference voltage.

13. The system as recited in claim 7, further comprising a pull-down transistor having a gate conductor and a source-to-drain current path, wherein the gate conductor is coupled to receive an output from the comparator and the source-to-drain current path is maintained during times when the reference voltage is maintained at approximately a midline voltage between the positive and negative voltage peaks of the output signal.

14. The system as recited in claim 13, wherein the comparator comprises a predefined slew rate and/or gain so that an output voltage from the comparator will not go below a threshold voltage of the pull-down transistor.

15. The system as recited in claim 7, further comprising an optical signal transmitter coupled to receive the output signal.

16. A method for regulating a duty cycle of an output signal, comprising presenting the output signal into a comparator for comparing the output signal to a predetermined reference voltage and feeding back the results of the comparison to a pull-down transistor that chops the output signal between a periodic and symmetric positive peak voltage value and the reference voltage, whereby the time at which positive peak voltage value extends above the reference voltage is directly proportional to the duty cycle of the output signal.

17. The method as recited in claim 16, wherein said presenting comprises connecting a positive input of a comparator to a conductor that receives the output signal and connecting a negative input of a comparator to a conductor that receives the reference voltage.

18. The method as recited in claim 16, wherein said feeding back comprises forwarding a voltage that remains above a threshold voltage of a pull-down transistor from the comparator to a gate conductor of the pull-down transistor to ensure the pull-down transistor is always active.

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19. The method as recited in claim 16, wherein said feeding back comprises chopping a negative-going waveform of the output signal to a steady state said reference voltage that, if variable, changes the pulse width and duty cycle of the output signal.

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